SOFTWARE-BASED MONITORING AND ANALYSIS OF A USB HOST CONTROLLER SUBJECT TO ELECTROSTATIC DISCHARGE

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INTRODUCTION

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I am a PhD candidate in computer engineering at the Missouri University of Science and Technology. My work focuses on modeling and metamodeling complex systems to understand and improve their dependability.

This research has been done in collaboration with Samsung, Ford, and the Missouri S&T Electromagnetic Compatibility Lab.
INTRODUCTION

- Static electricity discharge can cause:
  - Screen glitches
  - Program crashes
  - Erroneous software operation
  - System resets
  - Permanent hardware failures

- Dependable cyber-physical systems must be robust to the effects of these shocks

- The effects of these shocks on system hardware are much better understood than they are for software operation
MONITORING ESD

- Hardware instrumentation
  - Can provide a precise understanding of how Electro-Static Discharge (ESD) entered and propagated through the system
  - Is difficult to scale up to instrumentation for the whole system
  - Is infeasible to implement for field tests on commercially available equipment
  - Tests are often implemented using custom low-level software rather than a typical system software load

- Software instrumentation
  - Is often focused on user-visible faults such as display flicker and program crashes
  - Investigates lower-level faults, such as bit errors in registers, and is usually done with low-level code that cannot coexist with other software
  - The software executing on a system can affect its immunity to ESD
RESEARCH OBJECTIVES

- Improve software instrumentation for low-level faults
- Achieve software fault detection on consumer hardware in field use conditions
- Enable lightweight real-time monitoring and failure recovery
- Create a generic approach that applies to many system peripherals
- Validate and demonstrate by applying to USB devices
The **USB Host Controller** connects to the USB bus and performs low-level USB host device duties

**Responsibilities:**
- connecting and disconnecting devices
- configuring power delivery
- communicating control and data signals between the system’s memory and the USB devices
MONITORING APPROACH

- The Host Controller exposes a set of control registers to the host CPU
- These registers conform to Open Host Controller Interface specifications
- We record snapshots of these register values to approximate the HC’s internal operation, presuming that:
  - Certain sequences of values will be common during typical system operation
  - When exposed to ESD, we may observe anomalous values or sequences of values
- Our goal is to infer ESD exposure from anomalies in recorded traces of these snapshots
INITIAL INSTRUMENTATION APPROACH

- Directly read the memory-mapped Host Controller registers
- Modified an open-source tool, Myregrw, to suit our needs
  - System driver that reads memory addresses on command
  - User program that sends control signals to driver and records values
- Read values continuously while exposing the system to ESD
- Problem: register values remained mostly constant
- This approach failed to capture even typical Host Controller operation. Why?
INITIAL INSTRUMENTATION APPROACH

- We empirically determined the sampling rate of Myregrw on our system to be 342 Hz
- Assuming that, in the worst case, the register values change at 400 MHz, we have a 0.000856% chance of observing a given value
- Furthermore, Myregrw is racing the Host Controller driver to read the values written by the host controller before its driver overwrites them
- A new approach was needed to address both of these issues
IMPROVED INSTRUMENTATION APPROACH

- Instrument the USB Host Controller driver to record the register values at the start of each function
- Gives an exact picture of what the driver “sees” the host controller doing
- Requires minimal modifications to the driver code
- Values are recorded using the standard kernel logging framework
- Overhead is low: about 10% with a naive logging approach
ANALYSIS APPROACH

- Monitor system operation both without interference and while exposed to ESD
  - Baseline logs capture ‘normal’ system behavior without interference
  - ESD-exposed logs capture normal and abnormal system behavior
- These log files consist of sequences of snapshots of register values
- We refer to a log as an execution trace
- We refer to a snapshot of the registers’ values as a state
ANALYSIS APPROACH

- Identify and coalesce duplicate states in each trace to construct an execution graph
  - We also record the path through the graph taken by the execution trace

- Identify and coalesce duplicate states in each graph to construct a global execution graph
  - We ignore certain registers whose values are memory addresses set by the kernel memory allocator, as they do not reflect the operation of the Host Controller itself
  - Execution paths through the global graph are recorded for each trace

- We can then identify states and transitions unique to ESD-exposed execution traces
CASE STUDY

- System: FriendlyArm mini2440
  - 400 MHz ARM Samsung CPU
  - Running Linux as the operating system

- A flash drive is attached and a script runs to copy data to and from it

- Several ESD injections were performed:
  - Electric field coupling probe: ESD pulses between 500 V and 5.5 kV
  - Magnetic field coupling probe: ESD pulses between 500 V and 8 kV
  - The system proved to be more immune to magnetic field coupling, hence the higher pulse voltage
  - Probes were positioned over the USB port or the USB Host Controller IC
The HcInterruptEnable and HcInterruptDisable registers control whether the various hardware interrupts on the Host Controller are enabled or disabled.

When read, these registers ought to be duplicates of each other.

- Baseline data confirms the host controller follows this specification.
- However, under ESD exposure, slight dissimilarities are observed: bit 7 sometimes disagrees.

<table>
<thead>
<tr>
<th>Value</th>
<th>Baseline Probability</th>
<th>ESD-exposed Probability</th>
<th>Enable</th>
<th>Disable</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8000005e</td>
<td>0.22</td>
<td></td>
<td>0.20</td>
<td>0.20</td>
<td>0</td>
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<tr>
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<td></td>
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<td>0.66</td>
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<td>-0.00011</td>
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<tr>
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<td>0.0020</td>
<td></td>
<td>0.044</td>
<td>0.044</td>
<td>0</td>
</tr>
</tbody>
</table>
The **HcInterruptStatus** register records whether an interrupt has been triggered.

When exposed to ESD, we observe certain interrupts are more likely to be triggered:

- Frame number counter overflows (marked †)
- Hub status change events (marked *)

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**RESULTS: REGISTERS**
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- The HcControl register allows the Host Controller driver to control what the Host Controller processes next.

- Under ESD exposure, we observe:
  - Increased control frame processing (0x93) and decreased bulk data processing (0xa3).
  - Increased number of new control and data frames (0x83).
  - It is possible that ESD is disrupting the bus’s operation, resulting in more status change frames and more retransmissions of corrupted data frames.

![Graph showing change in probability and value probability for HcControl register values.

- Change in Probability: 0.14 0.12 0.1 0.08 0.06 0.04 0.02 0
- Values: 0x83 0x93 0xa3
- Value Probability: 1E-3 1E-2 1E-1 1E+0

Baseline vs ESD-exposed comparison.
The HcRhPortStatus0 register reports the status of the port we plugged the USB device into during tests.

Values where the port status remains unchanged (○) occur less often and port enable/disable events (†) occur more often.

Furthermore, port resets (*) are only observed in ESD-exposed traces.
The unified execution graph of two traces, one baseline and one ESD-exposed, is shown to the right.

Green states appear in baseline traces; red states appear only in ESD-exposed traces.

We see several potential effects of ESD:

1. Transitions from baseline states to non-baseline states
2. Transitions between non-baseline states
3. Transitions between baseline states not present in baseline traces
4. Transitions from non-baseline states to baseline states
We also observe differences in the distribution of state occurrences between baseline and ESD-exposed traces.

During normal operation, we expect to see:
- A large group of states revisited frequently — for example, the main control loop
- A short tail of ‘exceptional’ states that handle unusual events

If operation were disturbed by ESD, we would expect:
- Fewer common states
- A much longer tail of unusual or anomalous states

These assumptions are confirmed by our data.
CONCLUSIONS

- We have developed a methodology for studying the effects of ESD on system peripherals using software instrumentation.
- Our software probe records traces of a peripheral’s control registers.
- This approach approximates the unobservable internal behavior of the peripheral based on its behavior that is observable to the host CPU.
- The implementation has low overhead and can be used in field tests.
- We demonstrated this technique by applying it to a USB Host Controller.
- We were able to observe differences in system operation when the system was exposed to ESD.
CONCLUSIONS

• We can predict, based on the operation of the system, whether it has experienced the effects of ESD

• This allows us to identify which components on a system have experienced ESD and may require repair or better shielding

• Software may be able to determine that an ESD event has occurred and to automatically recover from resulting errors

• This would enable systems to continue operating in hostile environments

• We have determined that a naive classification approach can detect ESD events in a system execution trace with 88% accuracy

(work under review for IEEE Transactions on Electromagnetic Compatibility)
FUTURE WORK

- Expand this approach to other peripherals, enabling full-system monitoring of ESD effects
- Characterize the effects of ESD at specific injection locations, potentially allowing us to trace ESD through the board based on observed operation
- Develop software that can anticipate and recover from ESD events